

Docket No.: 060188-0820

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Sadami TAKEOKA, et al.	:	Confirmation Number: 5291
	:	
Application No.: 10/828,492	:	Group Art Unit: 2826
	:	
Filed: April 21, 2004	:	Examiner: DICKEY, Thomas L.
	:	
Patent No.: 7,348,595 B2	:	Issue Date: March 25, 2008
	:	
For: SEMICONDUCTOR DEVICE AND METHOD FOR TESTING SEMICONDUCTOR DEVICE		

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.322

Mail Stop Certificate of Correction
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reviewing the above-identified patent, a printing error was discovered therein requiring correction in order to conform the Official Record in the application.

The error noted is set forth on the two attached copies of form PTO-1050 Rev. 2-93 in the manner required by the Commissioner's Notice.

Specifically, on the Title page of the patent, in Item "(54)" the title of the application should be changed from "SEMICONDUCTOR WIRING SUBSTRATE, SEMICONDUCTOR DEVICE, METHOD FOR TESTING SEMICONDUCTOR DEVICE, AND METHOD FOR MOUNTING SEMICONDUCTOR DEVICE to --SEMICONDUCTOR DEVICE AND METHOD FOR TESTING SEMICONDUCTOR DEVICE--. In Item "(56) References Cited", change "2003/0008795 A1 01/2003 Asayama et al." to --2003/0006795 A1 01/2003 Asayama et al.--;

10/828,492

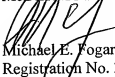
and change "2003/0032283 A1 02/2003 Nagao et al." to -- 2003/0032263 A1 02/2003 Nagao et al."--.

The change requested herein occurred as a result of printing the Letters Patent and the Certificate should be issued without expense under Rule 322 of the Rules of Practice. Attached, please find a copy of PTO Form 1449 which was filed on April 21, 2004, and a copy of the Amendment showing the above changes to the title, which was filed on December 20, 2005. Accordingly, Applicants request issuance of the Certificate of Correction.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Michael E. Fogarty
Registration No. 36,139

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Date: August 29, 2008

**Please recognize our Customer No. 53080
as our correspondence address.**

WDC99 1610324-1.060188.0820

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

PATENT NO : 7348595
APPLICATION NO. : 10/828,492
ISSUE DATE : March 25, 2008
INVENTOR(S) : Sadami TAKEOKA, et al.

Page 1 of 1

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title page, in Item "(54)" the title of the application, change "SEMICONDUCTOR WIRING SUBSTRATE, SEMICONDUCTOR DEVICE, METHOD FOR TESTING SEMICONDUCTOR DEVICE, AND METHOD FOR MOUNTING SEMICONDUCTOR DEVICE" to --SEMICONDUCTOR DEVICE AND METHOD FOR TESTING SEMICONDUCTOR DEVICE--;

In Item "(56) References Cited", change "2003/0008795 A1 01/2003 Asayama et al." to --2003/0006795 A1 01/2003 Asayama et al.--; and

change "2003/0032283 A1 02/2003 Nagao et al." to --2003/0032263 A1 02/2003 Nagao et al.--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

600 13th Street, N.W.
Washington, D. C. 20005-3096

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: ATTENTION Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277
 Sadami TAKEOKA, et al. : Confirmation Number: 5291
 Application No.: 10/828,492 : Group Art Unit: 2826
 Filed: April 21, 2004 : Examiner: DICKEY, Thomas L.
 For: A SEMICONDUCTOR DEVICE HAVING A DEVICE FOR TESTING THE SEMICONDUCTOR (AS AMENDED)

Mail Stop Amendment
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is an Amendment in the above-identified application.

- ☒ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	8	20	0	\$50.00 =	\$0.00
Independent Claims	4	4	0	\$200.00 =	\$0.00
Multiple dependent claims newly presented					\$0.00
Fee for extension of time					\$0.00
					\$0.00
Total of Above Calculations					\$0.00

- ☐ Please charge my Deposit Account No. 500417 in the amount of \$0.00. An additional copy of this transmittal sheet is submitted herewith.
- ☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

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 Phone: 202.756.8000 MEF:kap
 Facsimile: 202.756.8087
 Date: December 20, 2005

Please recognize our Customer No. 20277 as our correspondence address.



Docket No.: 060188-0820

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Sadami TAKEOKA, et al.	:	Confirmation Number: 5291
Application No.: 10/828,492	:	Group Art Unit: 2826
Filed: April 21, 2004	:	Examiner: DICKEY, Thomas L.

For: A SEMICONDUCTOR DEVICE HAVING A DEVICE FOR TESTING THE
SEMICONDUCTOR (AS AMENDED)

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated September 20, 2005, having a shortened statutory period for response set to expire December 20, 2005, please amend the above-identified application as follows:

Application No.: 10/828,492

AMENDMENTS TO THE TITLE

Please further amend the Title as follows:

~~A SEMICONDUCTOR DEVICE, AND METHOD FOR TESTING SEMICONDUCTOR~~
~~DEVICE HAVING A DEVICE FOR TESTING THE SEMICONDUCTOR~~

REMARKS

I. Introduction

Applicants have amended the Title of the Invention in accordance with the recommendation made by the Examiner in the Office Action. Applicants note with appreciation the indication of allowable subject matter being recited by claims 13 and 16.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection of Claims 11, 12, 14 and 15 Under 35 U.S.C. § 102

Claims 11, 12, 14 and 15 were rejected under 35 U.S.C. § 102 as being anticipated by Yamamura (U.S. 5,341,096). Applicants respectfully submit that Yamamura fails to anticipate the pending claims for at least the following reasons.

With regard to the present invention, claims 11 and 14 both recite, in-part, a semiconductor device comprising a *semiconductor wiring substrate* having a wiring layer.

In contrast to the claimed invention, Yamamura discloses an LSI mounted on a printed circuit board 6 (col. 2, lines 14-18, Fig. 5). However, it is clear that the printed circuit board is not a semiconductor substrate, and therefore cannot be deemed a semiconductor wiring substrate having a wiring layer. Thus, Yamamura fails to disclose at a minimum, a semiconductor device comprising a semiconductor wiring substrate having a wiring layer, as recited by the pending independent claims.

As anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), and at a minimum, Yamamura does not disclose a semiconductor device comprising a *semiconductor wiring substrate* having a wiring layer, it is clear that Yamamura does not anticipate either of claims 11 and 14, or any claim dependent thereon.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 11 and 14 are patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

IV. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication of which is respectfully solicited.

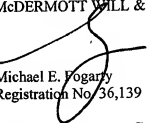
To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

Application No.: 10/828,492

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Facsimile: 202.756.8087
Date: December 20, 2005

**Please recognize our Customer No. 20277
as our correspondence address.**

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

 ATTY. DOCKET NO.
60188-820

 SERIAL NO.
Divisional of Appl. No.
10/187,269

 APPLICANT
Sadami TAKEOKA, et al.

 FILING DATE
April 21, 2004

GROUP

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 2002/0194564	12/2002	Tsuji et al.	
		US 6,519,728	02/2003	Tsuji et al.	
		US 6,400,173	06/2002	Shimizu et al.	
		US 2002/0171449	11/2002	Shimizu et al.	
		US 2003/0006795	01/2003	Asayama et al.	
		US 2003/0032263	02/2003	Nagao et al.	
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.